

Notice of References Cited

Application/Control No.

10/673,211

Applicant(s)/Patent Under
Reexamination
MONTAGNE ET AL.

Examiner

DIPAKKUMAR GANDHI

Art Unit

2117

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,745,372	04-1998	Fluegge, Michael W.	716/16
*	B	US-5,436,559	07-1995	Takagi et al.	324/158.1
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Harris et al., Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343.
	V	Venkatesan, Modelling Feedback Control Adjustment to Control Output Product Quality, Proceedings of American Control Conference, May 2002, vol. 6, Pages 5049-5053.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.